Docket No.: SON-2903
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Noboru Toyozawa et al.

Application No.: 10/541,092 | Confirmation No.: 4260

Filed: June 29, 2005 | Art Unit: 2629

For: DISPLAY DEVICE | Examiner: Yuk Chow

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

1. INTRODUCTORY COMMENTS

This is a Reply Brief under 37 C.F.R. §41.41 in response to the Examiner's Answer dated November 10, 2009.

Regarding any new issue raised in the Reply Brief, if present, U.S. patent practice and procedures set forth within 37 C.F.R. §41.43(a)(1) instructs as follows:

> After receipt of a reply brief in compliance with § 41.41, the primary examiner must acknowledge receipt and entry of the reply brief. In addition, the primary examiner may withdraw the final rejection and reopen prosecution or may furnish a supplemental examiner's answer responding to any new issue raised in the reply brief.

All arguments presented within the Appeal Brief of July 16, 2009 are incorporated herein by reference.

Additional arguments are provided hereinbelow.

2. ARGUMENTS

a. Page 7 of the Examiner's Answer contends that U.S. Patent No. 6,567,066 (Hashimoto) in Fig. 5 (VDD) reads on "supply voltage", and Fig. 6 (ΔV) offset voltage is charged at time of the rising edge of M1 (see Fig. 6, when M1 is switching on, and it is connected to VDD.)

In response, Figures 5 and 6 of Hashimoto are provided hereinbelow.

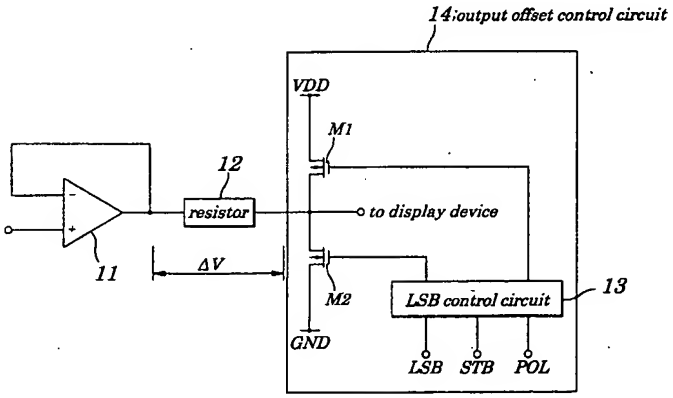


Figure 5

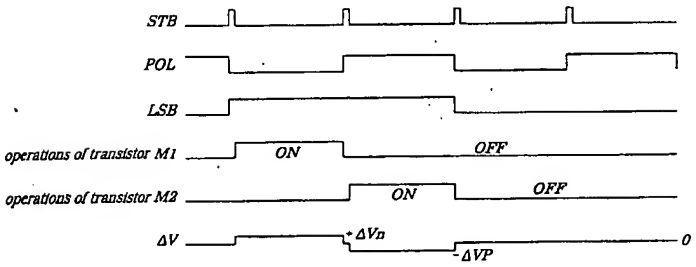


Figure 6

Claims 17 and 23-25 stand or fall together. Claims 23-25 are dependent upon claim 17. Independent claim 17 on appeal arguably discloses a display device *wherein said offset circuit is charged to an offset voltage at a time of a rising edge of a power supply voltage, said offset voltage adjusting a level of said common voltage.*

Hashimoto arguably discloses that a source of the **transistor M1** is connected to a terminal of ***supply voltage VDD*** and a source of the transistor M2 is connected to a ground GND. (Hashimoto at column 7, lines 15-18).

Hashimoto arguably discloses that to the LSB control circuit 13 are inputted the least significant bit (1 bit) of the digital image data and polarity signal POL and latch signal STB. (Hashimoto at column 7, lines 19-23). That is, an ***output offset control circuit 14*** is composed of transistors M1 and M2 and of the LSB control circuit 13. (Hashimoto at column 7, lines 23-24).

Hashimoto arguably discloses that if a resistance value of the resistor 12 including analog switches or the like is Rm, ***an offset voltage of $\Delta V = Im \times Rm$*** is generated due to a voltage drop and this voltage is added to the output voltage from the operational amplifier 11 and the total voltage is applied to the display device from the output terminal. (Hashimoto at column 7, lines 37-43).

Hashimoto arguably discloses that, therefore, a steady state current Im1 flows through the transistor M1 and, since the supply voltage VDD is supplied to a source of the transistor M1, a ***voltage rise*** of ***$\Delta Vn = Im1 \times Rm$*** occurs at the resistor 12. (Hashimoto at column 8, lines 28-33).

However, Figure 6 of Hashimoto ***fails*** to show a ***rising edge of supply voltage VDD***.

Page 7 of the Examiner's Answer contends that Hashimoto's Fig. 5 (VDD) reads on "supply voltage", and Fig. 6 (ΔV) offset voltage is charged at time of the rising edge of M1 (see Fig. 6, when M1 is switching on, and it is connected to VDD.).

In response, Hashimoto ***fails*** to disclose "M1" as being a voltage signal.

Instead, "M1" is disclosed within Hashimoto as being a "**transistor** M1". (Hashimoto at column 7, line 14).

Figure 5 of Hashimoto ***fails*** to show the supply voltage VDD being connected to the gate of transistor M1.

Instead, the transistors M1 and M2 are switched ON or OFF by the LSB control circuit 13 based on the least significant bit of the digital image data. (Hashimoto at column 7, lines 29-32).

Likewise, Figure 6 of Hashimoto ***fails*** to show a rising edge of the supply voltage VDD.

In this regard, Hashimoto ***fails*** to disclose ***supply voltage VDD*** and the ***operation of transistor M1*** as being one on the same.

As a consequence, Hashimoto fails to disclose, teach, or suggest the output offset control circuit 14 being charged to an offset voltage (ΔV) at a time of a rising edge of supply voltage VDD.

b. Page 7 of the Examiner's Answer contends that Hashimoto clearly shows this in Fig. 6, when at a time of falling edge of power supply voltage (when M1 is switching off), offset voltage ΔV is discharged to 0V.

In response, claim 18 stands or falls alone. Claim 18 is drawn to the display device as claimed in claim 17, wherein said offset circuit is discharged at a time of a falling edge of said power supply voltage.

As noted hereinabove, page 7 of the Examiner's Answer refers to *supply voltage VDD* of Hashimoto as the claimed "supply voltage".

Here, between the resistor 12 and the ***output terminal*** are connected transistors M1 and M2 drains of which are connected to each other. (Hashimoto at column 5, lines 13-15).

In this regard, a review of Figure 5 and 6 reveals that setting the ***operation of M1*** to an OFF state, while quite possibly disconnecting from supply voltage VDD from the output terminal, ***will not*** connect the output terminal to ground GND.

Moreover, Figure 6 of Hashimoto ***fails*** to show a falling edge of the supply voltage VDD.

As a consequence, Hashimoto fails to disclose, teach, or suggest that the output offset control circuit 14 is discharged at a time of a falling edge of the supply voltage VDD.

c. Page 7 of the Examiner's Answer contends that U.S. Patent No. 6,313,819 (Maekawa) teaches a source follower circuit is constructed with a polysilicon TFT (Col. 4 line 18), and it's a well known process in the art that the presence of an insulating substrate in polysilicon TFT fabrication.

In response, claim 19 stands or falls alone. Claim 19 is drawn to the display device as claimed in claim 18, wherein said matrix of pixels, said offset circuit, and said start circuit are mounted on an insulating substrate.

In response, Maekawa is ***silent*** as to the presence of an insulating substrate.

Nevertheless, the Examiner's Answer asserts that it's a well known process in the art that the presence of an insulating substrate in polysilicon TFT fabrication.

As a reply to the assertion of what is "*well known*", there is no concession as to the veracity of Official Notice taken in the Examiner's Answer.

Instead, U.S. patent practice and procedures pursuant to 37 C.F.R. §1.104(d)(2) dictate the following:

> When a rejection in an application is based on facts within the personal knowledge of an employee of the Office, the data shall be as specific as possible, and the reference **must be supported**, when called for by the applicant, by the affidavit of such employee, and such affidavit shall be subject to contradiction or explanation by the affidavits of the applicant and other persons.

The Appellant requests an affidavit or document in support of the assertion in the Examiner's Answer that *the presence of an insulating substrate in polysilicon TFT fabrication is well known.* 37 C.F.R. §1.104(d)(2), M.P.E.P. §2144.03.

In this regard, failure to provide any objective evidence to support the challenged use of Official Notice constitutes ***clear and reversible error***. *Ex parte Natale*, 11 USPQ2d 1222, 1227-1228 (Bd. Pat. App. & Int. 1989).

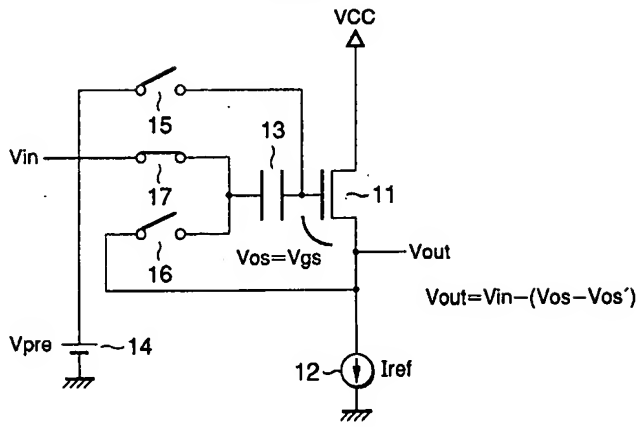
Thus, Hashimoto and Maekawa, either individually or as a whole, fail to disclose, teach, or suggest a display device wherein the matrix of pixels, the offset circuit, and the start circuit are mounted on an insulating substrate.

d. Page 7 of the Examiner's Answer contends that regarding claim 20, Maekawa clearly teaches the coupling capacitor is not mounted on said insulating substrate (see Fig. 2(14) and Col. 4 lines 6-15).

In response, claim 20 stands or falls alone. Claim 20 is drawn to *the display device as claimed in claim 19, wherein said coupling capacitor is mounted on another substrate other than said insulating substrate.*

Figure 2 of Maekawa is provided hereinbelow.

FIG.2



Here, Figure 2 of Maekawa ***fails*** to show the presence of an insulating substrate.

Maekawa at column 4, lines 6-15, is provided hereinbelow.

> In addition, it is not necessary to make output impedance of the signal source extremely small because precharging of the capacitor 13 can be carried out by the independent precharge supply 14 rather than by a signal source. This has great benefits when this source follower circuit is used as an output circuit for a reference voltage selection type DA converter within a horizontal driver of a liquid crystal display device. Namely, the line width of the reference voltage line can be made small, so that the whole circuit can be formed in a small area.

Here, column 4, lines 6-15, of Maekawa ***fails*** to show the presence of an insulating substrate.

Thus, Hashimoto and Maekawa, either individually or as a whole, fail to disclose, teach, or suggest a display device wherein said coupling capacitor is mounted on another substrate other than said insulating substrate.

e. Page 8 of the Examiner's Answer contends that regarding claim 21, Maekawa teaches a start circuit (Fig. 2(15-17)) and start circuit charging a coupling capacitor (see Col. 3 lines 23-55).

In response, claim 21 stands or falls alone. Claim 21 is drawn to *the display device as claimed in claim 18, wherein said common driver has a start circuit, said start circuit charging a coupling capacitor within said offset circuit to said offset voltage.*

Hashimoto ***fails*** to show the presence of a capacitor within the output offset control circuit 14.

Maekawa arguably discloses that the gate of the source follower transistor 11 is connected to one end of a capacitor 13. (Maekawa at Figure 2, column 3, lines 27-28).

However, Maekawa ***fails*** to disclose the capacitor 13 within an offset circuit.

Thus, Hashimoto and Maekawa, either individually or as a whole, fail to disclose, teach, or suggest a display device wherein said common driver has a start circuit, said start circuit charging a coupling capacitor within said offset circuit to said offset voltage.

f. Page 8 of the Examiner's Answer contends that regarding claim 22, Maekawa teaches the start circuit only operates during a precharge period (see Col. 3 lines 46-64), hence being in a non-operational state during other time.

In response, claim 22 stands or falls alone. Claim 22 is drawn to *the display device as claimed in claim 21, wherein said start circuit operates only at the time of the rising edge of the power supply voltage and at the time of a falling edge of the power supply voltage, said start circuit being in a non-operational state during other times.*

Maekawa arguably discloses that in the first embodiment in FIG. 2, a source follower circuit has an NMOS source follower transistor 11 connected to a **power supply VCC** with the drain thereof and a current source 12 connected across the source of the source follower transistor 11 and earth (Maekawa at Figure 2, column 3, lines 23-27).

Figures 2 and 3 of Maekawa are provided hereinbelow.

FIG.2

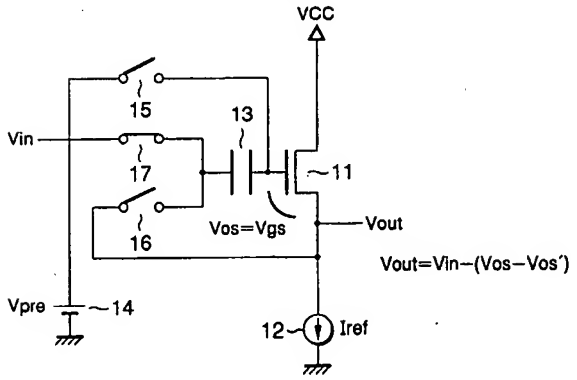
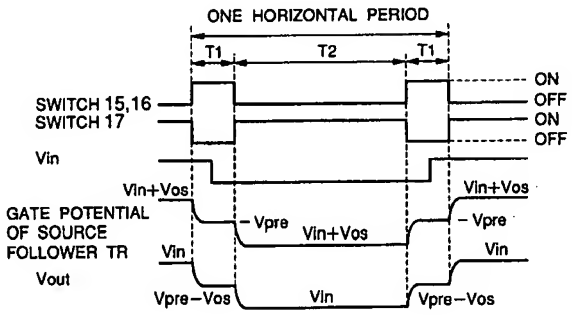


FIG.3



Here, Figures 2 and 3 of Maekawa ***fail*** to depict the presence of a start circuit that only operates during a precharge period.

Thus, Hashimoto and Maekawa, either individually or as a whole, fail to disclose, teach, or suggest a display device wherein said start circuit operates only at the time of the rising edge of the power supply voltage and at the time of a falling edge of the power supply voltage, said start circuit being in a non-operational state during other times.

g. Page 8 of the Examiner's Answer contends that regarding claim 26, the disclosure of U.S. Patent No. 6,091,391 (Ling) suggests that driving of display area being prohibited in standby mode (Col. 3 line 23-24, "DAC 130 input is set to zero so that it consumes zero current", this indicates that driving of the display is suspended since the DAC input is set to zero current).

In response, claim 26 stands or falls alone. Claim 26 is drawn to an electronic device capable of switching between a normal power consumption state and a low power consumption state, the electronic device comprising:

> the display device as claimed in claim 17, the matrix of pixels being within a display area; and
>
> a panel having a peripheral circuit and said display area, said panel being switchable between an operational mode and a standby mode;
>
> wherein power consumption by said panel in said operational mode is higher than in said standby mode, driving of said display area being prohibited in said standby mode.

Here, no timing diagram can be found within Ling.

The Examiner's Answer cites column 3, lines 23-24, of Ling.

In this regard, Ling arguably discloses that during the IDLE cycle, the R2R DAC 130 input is set to zero so that it consumes zero current, and the capacitor is fully charged to VREF voltage. (Ling at column 3, lines 23-24).

Nevertheless, Ling ***fails*** to disclose, teach, or suggest driving of the display area being prohibited in the standby mode.

Thus, Hashimoto and Ling, either individually or as a whole, fail to disclose, teach, or suggest an electronic device wherein power consumption by said panel in said operational mode is higher than in said standby mode, driving of said display area being prohibited in said standby mode.

3. CONCLUSION

The prior art of record fails to disclose, teach or suggest all the features of the claimed invention.

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

For at least the reasons set forth hereinabove, the rejection of the claimed invention should not be sustained. Therefore, a reversal of the rejection is respectfully requested.

If any additional fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: December 8, 2009

Respectfully submitted,

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